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EXAMINER	
BATAILLE, PIERRE MICHE	
ART UNIT	**PAPER NUMBER**
2186	18

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,229	WARD, WILLIAM P.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *2 and 3* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-26,28,30-33,40,41 and 44* is/are rejected.

7)☒ Claim(s) *27,29,34-39,42 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. This Office Action is taken in response to Applicant's communication filed October 20, 2003 in response to Office Action/Rejection dated July 17, 2003. The Applicant's arguments and/or amendments have been considered with the results that follow.

2. Claims 1-23 were originally presented in the application under examination. Of the original claims, claims 2-3 have been canceled, claims 24-30 have been previously added in previous amendment and claims 31-44 have been newly added.

Response to Arguments

3. Applicant's arguments filed October 20, 2003 with respect to claims 1 and 4-44 have been fully considered but they are not deemed to be persuasive for at least the remarks below.

Claim 1 has been amended to recite that the memory controllers are allocated to respective time slots according to a predetermined priority scheme. Applicant adds that Welker's memory controller (US 6,076,139) does not need to perform arbitration for the Ram bus channel since there is one controller connected per Rambus channel. However, not only this is a principle of Rambus controller ("A Memory Controller For Access Interleaving Over A Single Rambus", used for reference only, discusses general principle of Rambus Memory Controller), Welker's memory controllers perform

arbitration for the Rambus channel. Interleaving capability of the Rambus Channel Access interleaving is inherently supported in the Rambus protocol and Access Interleaving on Rambus memory controller is the scheduling algorithm. When a request results in a miss, the transaction is completed at the end of the acknowledge window and the master would have to wait for the Read/Write MissDelay cycles before reissuing the request. Section 2.2 discusses access interleaving and how it effects on memory controller where the controller must ensure that there will be no conflicts on the Rambus channel by scheduling the requests and data packets in proper bus cycles. For a new request issued in the middle of some previous transaction, the controller should know the state of the Rambus channel: which time slots are free and which are reserved.

Welker's memory controller is no exemption from these principles. Welker teaches time slot priority scheme corresponding to the disclosed channel priority scheme, a well known principle of Rambus channel wherein no master can write to a channel until another master write is completed [Col. 7, Lines 53-57; Col. 5, Lines 26-29]. Welker at least implicitly teaches the claimed time slot priority scheme because of the disclosed interleaved transactions where write cycles to a channel (i.e. 2) is used while a previous write to another channel (i.e. 1) is not yet completed and because a lock attempt to channel 1 is held or placed in a queue or is assigned a priority timing (slot) until the previous write to the channel (1) is completed [Col. 5, Lines 23-62; Col. 8, Lines 16-30]. Welker teaches accesses to be completed out of order with a highest priority access or read requests may take priority over write requests and processor or other master having write highest priority on selected slot or channel (Col. 8, Lines 16-

35; Col. 5, Lines 26-34)]. In view of the above, it is clear that access priority scheme is suggested by Welker, the priority scheme defining time slot allocated to respective MIC controller. Such teaching is combinable with Cohen (US 6,026,464) describing a request/grant arbitration scheme enabling different memory controller to access the bus.

With respect to claim 10, applicant argues that neither reference teaches "a hub that is connected to a plurality of memory buses where each memory controller to monitor memory requests generated by another memory controller in performing related memory actions. Again, Walker identifies Rambus channels (synchronous, high speed Rambus channel 202-208, Fig. 2) indicating each Rambus controller as either a master controller or a slave controller, the master and slave controller identify a plurality of memory controllers or memory interface control (MIC) blocks connected to the memory bus each MIC controller including its own snoop controller for generating snoop cycles and return snoop transactions response which the requesting controller acknowledges in performing memory related actions or snoop accesses, memory read/write, read-modify write [Col. 4, Lines 37-54; Col. 5, Lines 15-45; Col. 8, Line 58 to Col. 9, Line 20].

Again this is a principle of the modified Rambus which has been modified by using a separate BusCtrl line for each slave where only one slave see the beginning of the request packet while the other slaves keep monitoring the bus for new requests. (Section 2.1.1 "A Memory Controller For Access Interleaving Over A Single Rambus"). The reference further suggests that the Rambus channel can be expanded by attaching

one or more Rambus channels via a transceiver forming an interleaved memory system (section 1.2.2).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4-9, 23-25, 30-32, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,076,139 (Welker et al) in view of US 6,026,464 (Cohen).

As per claim 1, Welker shows a system (as shown in Fig. 1 and 2) comprising: a memory bus (*multi-channel memory interface 106, Fig. 1; synchronous, high speed Rambus channel 202-208, Fig. 2*) [Col. 3, Lines 31-38]; and a plurality of memory controllers (*memory interface control (MIC) blocks 310, Fig. 3*) [Col. 4, Lines 37-39], (each MIC 310 is coupled to the bus masters 212-220 through a single address, data and control bus 314, i.e. to the single bus are attached a plurality of MIC or memory controllers) [Col. 7, Lines 43-44]; each memory controller to generate memory requests on the memory bus, at least two of the memory controllers are adapted to generate concurrently pending memory requests on the memory bus (*each memory controller running memory cycles from their respective masters*) [Col. 4, Lines 39-49] according to a priority scheme [Col. 4, Lines 51-54; Col. 8, Lines 16-19]. Welker teaches the system wherein the predetermined priority scheme comprises a time slot priority scheme (*time slot priority scheme corresponds to the disclosed channel priority scheme, a well known*

principle of Rambus channel wherein no master can write to a channel until another master write is completed) [Col. 7, Lines 53-57; Col. 5, Lines 26-29]. Welker at least implicitly teaches the claimed time slot priority scheme because of the disclosed interleaved transactions where write cycles to a channel (i.e. 2) is used while a previous write to another channel (i.e. 1) is not yet completed and because a lock attempt to channel 1 is held or placed in a queue or is assigned a priority timing (slot) until the previous write to the channel (1) is completed [Col. 5, Lines 23-62; Col. 8, Lines 16-30]. Although Welker further discloses multiple channel controller provide concurrent access to memory 132 [Col. 3, Line 41], the applicant is not convince that the claimed feature "at least two of the plurality of memory controllers are adapted to generate concurrently pending memory requests on the memory bus" is anticipated by Welker. However, Cohen uses distributed memory controllers for memory access wherein each of the memory controllers monitors bus access by all the other memory controllers [abstract; Col. 1, Lines 57-58; Col. 3, Lines 44-47]; each of the distributed memory controllers can perform independent memory accesses in parallel with other memory controllers [Col. 2, Line 28-29]. Therefore, it would have been obvious to one having ordinary skill in the art, and having both teachings before him at the time of the invention to provide distributed memory controller, as taught by Cohen because the distributed memory controllers would have enabled the maximum number of memory banks to be used at all times [Col. 1, Line 61-67]. The combination is proper because Cohen teaches distributed memory control prevents a single device from dominating or creating a bottleneck in the global memory

system and increases utilization of the global memory by overlapping memory accesses [Col. 2, Line 1-5].

As to claim 23, Welker discloses the invention as claimed, monitoring requests from another controller on a memory bus and determining if a memory request can be generated on the memory bus based on the monitoring, as details above with respect to claims 1-22 (see Col. 4, Lines 50-54; Col. 5, Lines 26-29; Col. 8, Lines 58-66); Welker does not specifically discloses an article of manufacture comprising one or more storage media containing instructions when executed to cause the memory controller implement the control functions, as noted above. However, one having ordinary skill in the art would have recognized that it is well known in the art that computer storage medium (i.e. floppy, CD-ROM, etc.) carry computer executable instructions because it would facilitate transporting and installing executable instruction on other systems. For example, a copy of Microsoft Windows Operating system software is carried on a CD-ROM from which Windows operating system can be installed onto other system, which is a lot easier than running a long cable to install the operating system from a network based server. Therefore, it would have been obvious to one having ordinary skill in the art, to put Welker's control system and method on designed instructions to be carried on a computer storage media, because it would have facilitated the transporting, installing and implementing of Welker's method on other systems.

As to claim 4, Welker teaches the memory bus comprising a Rambus channel (*system bridge 106 is a multi-channel memory interface 200 which provides multiple Rambus or memory channel 202-208*) [Col. 3, Lines 31-39].

As per claims 6, Welker discloses the system wherein the memory bus comprises plural control portions (*memory interface control blocks 310, Fig. 3*) [Col. 4, Lines 37-39], each of the control portions associated with corresponding priority scheme (*memory control block 310 running memory cycles from their respective masters or processor assigned a predetermined priority on predetermined channel*) [Col. 8, Lines 16-30].

As per claim 9, Welker discloses the system wherein each of the memory bus comprises plural portions (*memory interface control channel 0-3*), each portion associated with a set of memory devices (*Rambus dynamic random access memory (RDRAM)*) [Fig. 2; Col. 3, Lines 33-40; Col. 4, Lines 55-58; Col. 7, Lines 33-37].

As per claim 5, Welker discloses the system wherein each memory controller generates a memory request during a different predetermined time slot (*one snoop request at a time where a central arbiter prioritizes snoop requests*) [Col. 5, Lines 26-34; Col. 8, Lines 58-61].

As per claim 7, Welker discloses the system wherein the time slot priority scheme are staggered [*interleaved transactions are assigned or arranged in round-robin fashion on selected channel select* (Col. 8, Lines 16-29)].

As per claims 8, Welker discloses the system wherein the control portions comprise a row portion and a column portion (*a well known principle of Rambus channel, well known principle of interleaving in Rambus channel, and embedded feature of the memory channel in Welker because row accesses separated from column accesses over separated row access pins and column access control pins would provide interleaved transactions, as Welker's system features interleaved transactions over RAMBUS channel to control performance gained*) [Col. 3, Lines 48-55;

Col. 8, Lines 8-30]; Walker's system handles separate row and column accesses simultaneously [Col. 3, Lines 46-55].

As per claims 24-25, 30, and 44, Welker teaches the memory controllers connected to the memory bus (*the memory controller carry memory control information over the channels*) at least two of the memory controllers are adapted to generate concurrently pending memory requests on the memory bus or at least two memory controllers adapted to generate its memory requests (snoop arbiter (312, Fig. 3, and 702, Fig. 7) to receive individual snoop requests from each memory channel to determine snoop cycle priority when processor contending for the same channel with another master implementing read and write accesses, and read-modify-write accesses) [Col. 2, Line 66 to Col. 3, Line 5; Col. 5, Lines 46-64; Col. 7, Lines 24-26]. Welker further discloses the system wherein the control portions comprise a row portion and a column portion (*a well known principle of Rambus channel, well known principle of interleaving in Rambus channel, and embedded feature of the memory channel in Welker because row accesses separated from column accesses over separated row access pins and column access control pins would provide interleaved transactions, as Welker's system features interleaved transactions over RAMBUS channel to control performance gained*) [Col. 3, Lines 48-55; Col. 8, Lines 8-30]; Walker's system handles separate row and column accesses simultaneously [Col. 3, Lines 46-55]; the system wherein the predetermined priority scheme comprises a time slot priority scheme (*time slot priority scheme corresponds to the disclosed channel priority scheme, a well known principle of Rambus channel wherein no master can write to a channel until another master write is completed*) [Col. 7, Lines 53-57; Col. 5, Lines 26-29].

With respect to claims 31-32, Welker teaches the system wherein the predetermined priority scheme comprises a time slot priority scheme (*time slot priority*

scheme corresponds to the disclosed channel priority scheme, a well known principle of Rambus channel wherein no master can write to a channel until another master write is completed) [Col. 7, Lines 53-57; Col. 5, Lines 26-29].

6. Claims 10-22, 26, 28, 33, and 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,076,139 (Welker et al) in view of US 6,026,464 (Cohen), and further in view of "A Memory Controller For Access Interleaving Over A Single Rambus" (Xanthaki).

As per claims 10, 33, and 40, Welker discloses a system (as shown in Fig. 1 and 2) comprising: a memory bus (*multi-channel memory interface 106, Fig. 1; synchronous, high speed Rambus channel 202-208, Fig. 2*) [Col. 3, Lines 31-38]; and a plurality of memory controllers (*memory interface control (MIC) blocks 310, Fig. 3*) connected to the memory bus [Col. 4, Lines 37-39], each memory controller to monitor memory requests generated by another memory controller (*each MIC controller includes its own snoop controller 706 generating snoop cycles and return snoop transactions response which the requesting controller acknowledges*) [Col. 4, Lines 50-54; Col. 8, Line 58 and Col. 9, Line 20] in performing memory related actions (*snoop accesses, memory read/write, read-modify write*) [Col. 5, Lines 15-45]. Although Welker further teaches each MIC controller includes its own snoop controller generating snoop cycles and returns snoop transactions response, and snooping (see Class Definition 711/146) is defined as monitoring an associated address bus to determine if access to a cached location occurs by another cache memory or other user (e.g., DMA, peripherals, etc.); the applicant is not convince that the claimed feature "each memory

controller to monitor memory requests generated by another memory controller in performing memory related transaction" is taught by Welker. However, Cohen uses distributed memory controllers for memory access wherein each of the memory controllers monitors bus access by all the other memory controllers [abstract; Col. 1, Lines 57-58; Col. 3, Lines 44-47]; each of the distributed memory controllers can perform independent memory accesses in parallel with other memory controllers [Col. 2, Line 28-29]. Neither reference explicitly teaches a hub connected to the memory buses and the plurality of memory controllers. However, Xanthaki explicitly states this feature to be a well known principle of Rambus memory controller, as Rambus channel can be expanded by attaching one or more Rambus channels via a transceiver forming an interleaved memory system (section 1.2.2). Therefore, it would have been obvious to one having ordinary skill in the art, and having both teachings before him at the time of the invention to provide distributed memory controller, as taught by Cohen because the distributed memory controllers would have enabled the maximum number of memory banks to be used at all times [Col. 1, Line 61-67]. The combination is proper because Cohen teaches: distributed memory control prevents a single device from dominating or creating a bottleneck in the global memory system and increases utilization of the global memory by overlapping memory accesses [Col. 2, Line 1-5].

As per claims 11 and 41, Welker discloses the memory related actions to comprise read-modify-write action [Col. 5, Lines 36-40].

As per claim 12, Welker discloses the memory related actions to comprise a cache coherency action [Col. 5, Lines 26-40].

As per claim 13, Welker discloses the memory related actions to comprise a memory request (memory read and write requests) [Col. 4, Lines 1-4; Col. 5, Lines 20-40; Col. 6, Lines 19-24].

As per claims 14, Welker discloses the memory controller to determine if the memory bus is available based on outstanding requests from other memory controllers (*central snoop arbiter to receive individual snoop requests from each memory channel to determine snoop cycle priority when processor contending for the same channel with another master implementing read and write accesses*) [Col. 2, Line 66 to Col. 3, Line 5; Col. 5, Lines 46-64; Col. 7, Lines 24-26].

As per claim 15, Walker discloses a system (as shown in Fig. 1 and 2) implemented a method providing a plurality of memory controllers (*memory interface control (MIC) blocks 310, Fig. 3*) [Col. 4, Lines 37-39] on a memory bus (*multi-channel memory interface 106, Fig. 1; synchronous, high speed Rambus channel 202-208, Fig. 2*) [Col. 3, Lines 31-38]; the memory controllers generating requests on the memory bus (*each memory controller running memory cycles from their respective masters*) [Col. 4, Lines 39-49]; and each memory controller monitoring memory requests generated by another memory controller (*each MIC controller includes its own snoop controller 706 generating snoop cycles and return snoop transactions response which the requesting controller acknowledges*) [Col. 4, Lines 50-54; Col. 8, Line 58 and Col. 9, Line 20] in performing memory related actions (*snoop accesses, memory read/write, read-modify write*) [Col. 5, Lines 15-45]. Cohen uses distributed memory

controllers for memory access wherein each of the memory controllers monitors bus access by all the other memory controllers [abstract; Col. 1, Lines 57-58]; each of the distributed memory controllers can perform independent memory accesses in parallel with other memory controllers [Col. 2, Line 28-29; Col. 3, Lines 44-47]. Therefore, it would have been obvious to one having ordinary skill in the art, and having both teachings before him at the time of the invention to provide distributed memory controller, as taught by Cohen because the distributed memory controllers would have enabled the maximum number of memory banks to be used at all times [Col. 1, Line 61-67]. The combination is proper because Cohen teaches distributed memory control prevents a single device from dominating or creating a bottleneck in the global memory system and increases utilization of the global memory by overlapping memory accesses [Col. 2, Line 1-5].

As per claim 16, Walker discloses generating the requests comprising generating Rambus command packets (*packet type data received and transmitted from and to Rambus DRAM (RDRAMs) by a transaction protocol according to the Rambus channel*) [Col. 7, Lines 53-63].

As per claims 17, Walker discloses generating the requests comprising the memory controllers generating the requests one at a time according to predetermined priority scheme (*one snoop request at a time where a central arbiter prioritizes snoop requests*) [Col. 5, Lines 26-34; Col. 8, Lines 58-61].

As per claim 18, Welker teaches generating the requests according to a time slot priority scheme (*time slot priority scheme corresponds to the disclosed channel priority scheme, a well*

known principle of Rambus channel wherein no master can write to a channel until another master write is completed) [Col. 7, Lines 53-57; Col. 5, Lines 26-29]. Welker at least teaches the claimed time slot priority scheme because of the disclosed interleaved transactions where write cycles to a channel (i.e. 2) is used while a previous write to another channel (i.e. 1) is not yet completed and because a lock attempt to channel 1 is held or placed in a queue or is assigned a priority timing (slot) until the previous write to the channel (1) is completed [Col. 5, Lines 23-62; Col. 8, Lines 16-30].

As per claim 19, Welker discloses generating the requests according to a request-select priority scheme [*accesses may be completed out of order with a highest priority access* (Col. 5, Lines 19-34) *and processor or other master having write highest priority on selected channel* (Col. 8, Lines 16-29)].

As per claim 20, Welker discloses each memory controller determining when to generate a memory request based on the monitoring (*receiving snoop requests from a plurality of sources and determining priority among the snoop requests received and granting highest priority to one of the snoop requests*) [Col. 5, Lines 26-29; Col. 8, Lines 58-61].

As per claim 21, Welker discloses each memory controller determining if a lock has been asserted due to the presence of a read-modify-write transaction [Col. 5, Lines 29-40].

As per claim 22, Welker discloses each memory controller (*each memory control block (MIC) comprises page hit detector-controller 712*) performing a cache coherency action based on the monitoring (*snoop action or page hit*) [Col. 7, Line 64 to Col. 8, Line 12; Col. 8, Line 67 to Col. 9, Line 31].

As per claims 26 and 28, Welker teaches the memory controllers connected to the memory bus (*the memory controller carry memory control information over the channels*) at least two of the memory controllers are adapted to generate concurrently pending memory requests on the memory bus or at least two memory controllers adapted to generate its memory requests (snoop arbiter (312, Fig. 3, and 702, Fig. 7) to receive individual snoop requests from each memory channel to determine snoop cycle priority when processor contending for the same channel with another master implementing read and write accesses, and read-modify-write accesses) [Col. 2, Line 66 to Col. 3, Line 5; Col. 5, Lines 46-64; Col. 7, Lines 24-26].

Allowable Subject Matter

7. Claims 27, 29, 34-39, and 42-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Pierre-Michel Bataille
Examiner
Art Unit 2186

December 6, 2003